

CURRENT CAPABILITY OF VSUP AND VAUX[2:0]

Product Family: **EM85xx**

Part Number: EM8500, EM8502, EM8504

Keywords: Power management, Energy harvesting, Solar, TEG, MPPT, Configuration, Setup, Super capacitors, Secondary Battery, Primary Battery

NOTIFICATION

The EM85xx naming shall be used in this document as a generic part number name for EM85xx devices.

ABSTRACT

The EM85xx offers a NVM containing all the configuration parameters. This document describes how to setup the registers linked to output drive capability of the supplies VSUP and VAUX[2:0] used without LDO in the NVM

ABBREVIATIONS

| | |
|-------------------------|--|
| NVM | Non-Volatile-Memory |
| MCU | Microcontroller Unit |
| STS | Short term storage element (capacitor connected to VDD_STS) |
| LTS | Long term storage element (rechargeable battery connected to VDD_LTS) |
| HRV | Harvester, main source of energy (solar or TEG) |
| TEG | Thermoelectric Generator |
| VLD | Voltage Level Detector |
| Vref | Voltage level detector reference level |
| Vlvl | Voltage level detector LSB (71.88mV) |
| Vbat | Battery voltage connected to VDD_LTS |
| VSUP | Main output supply for application |
| VAUX[i] | 2 independent auxiliary supplies for application |
| R _{BAT} | Battery internal resistivity |
| R _{SW_LTS_STS} | STS to LTS switch resistivity |
| R _{SW_VSUP} | STS to VSUP switch resistivity |
| R _{SW_VAUXi} | STS to VAUXi switch resistivity |
| I _{TOT} | Total current flowing from LTS to VSUP and/or VAUXi |
| I _{STD} | Total current flowing from LTS to VSUP and/or VAUXi in normal mode (low power) |
| I _{PEAK} | Total current flowing from LTS to VSUP and/or VAUXi in high mode |

1 SCOPE

The EM85xx delivers 4 output supplies:

1. VSUP: main supply output usually used for MCU
2. VAUX[2:0]: 3 supply outputs used for peripherals such as RF, sensors, actuator etc...
 Each supply output can be directly connected to STS or regulated. When the LDO is used, the maximum current the EM85xx can deliver is limited by the LDO drive capability. This document describes the way to configure the device when VSUP and/or VAUX[2:0] are directly connected to STS.

The following registers are involved for that action:

| Register name | Address | Description |
|----------------------|---------|---|
| reg_v_bat_min_hi_con | 0x0A | Minimum battery and application voltage when STS and LTS are connected, form an hysteresis with v_bat_min_lo |
| reg_v_bat_min_lo | 0x0B | Absolute minimum value of the battery and the application |
| reg_v_apl_max_hi | 0x0C | Absolute maximum application voltage (ignored if set to 0xFF) |
| reg_v_apl_max_lo | 0x0D | Maximum application voltage low level of hysteresis (ignored if set to 0xFE) |
| reg_ldo_cfg | 0x0E | Configuration of the LDO |
| reg_vaux_cfg | 0x10 | Configuration of VAUX[2:0] |

Table 1: List of Registers Related to Maximum Current Driven on VSUP and VAUX

The default value after reset or start-up of the registers listed in [Table 1](#) is contained in a NVM memory at the following related addresses:

| Register name | Register Address | Related address in NVM | |
|-----------------------------|------------------|------------------------|------|
| <i>reg_v_bat_min_hi_con</i> | 0x0A | eprom10 | 0x4A |
| <i>reg_v_bat_min_lo</i> | 0x0B | eprom11 | 0x4B |
| <i>reg_v_apl_max_hi</i> | 0x0C | eprom12 | 0x4C |
| <i>reg_v_apl_max_lo</i> | 0x0D | eprom13 | 0x4D |
| <i>reg_ldo_cfg</i> | 0x0E | eprom14 | 0x4E |
| <i>reg_vaux_cfg</i> | 0x10 | eprom16 | 0x50 |

Table 2: Mapping of Registers in EEPROM

Note: the offset between the register addresses and related address in NVM is 0x40

2 DISABLE THE LDO

2.1 VSUP LDO

This part describes the way to configure the EM85xx devices, when no LDO is used. There are two conditions to keep the LDO on VSUP always disabled:

1. Set the register `reg_ldo_cfg.frc_ulp_ldo = '0'`
2. The voltage on STS shall be always lower than `v_apl_max_lo`

The easiest way to ensure that STS is always lower than `v_apl_max_lo` is to configure the device as follows:

`reg_v_apl_max_hi = 0xFF`
`reg_v_apl_max_lo = 0xFE`

2.2 VAUX LDO

To ensure the VAUX LDO is always disabled, the device shall be configured as follows:

`reg_vaux_cfg = 0x00`

3 CURRENT FLOW

The storage elements STS and LTS are considered as connected in that description. It is not recommended to drive high current on VSUP and VAUX when STS and LTS are disconnected.

The current flows from the battery to VSUP and VAUX as follows:

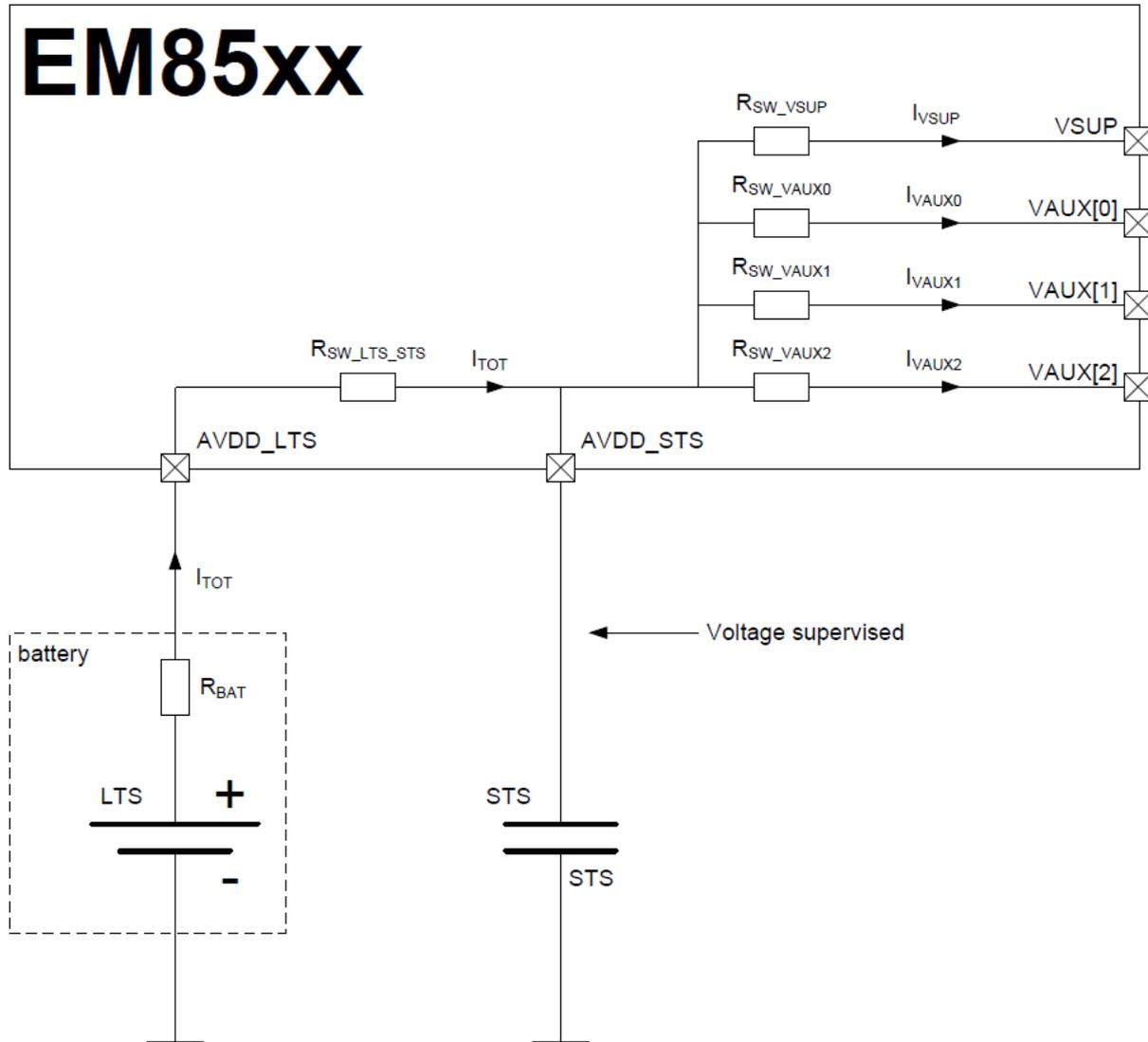


Figure 1: Current Flow Diagram

The current driven on VSUP and/or VAUX will generate a voltage drop on LTS and STS due to the different switches resistivity.

When STS and LTS are connected the EM85xx supervises STS.

When STS is detected lower than `v_bat_min_lo`, it disables VSUP and VAUX[2:0] to protect the system against overload.

4 REGISTER V_BAT_MIN_HI_CON CALCULATION

We consider 2 current levels:

1. Standard current I_{std} : total current load on VSUP and VAUX[2:0] in normal mode
2. Peak current I_{peak} : total peak current load on VSUP and VAUX[2:0] in high consumption mode

We consider the following worst case scenario:

The total charge current I_{TOT} is the sum of currents loaded on VSUP and VAUX[2:0].

The EM85xx is in normal mode and therefore $I_{TOT} = I_{std}$. The worst case is considered here – STS = $v_bat_min_hi_con$ at the moment the current peak I_{peak} is driven on VSUP and/or VAUX[2:0]. The voltage on LTS and STS drops but shall remain above $v_bat_min_lo$ to keep the system working.

The following timing diagram illustrates this scenario:

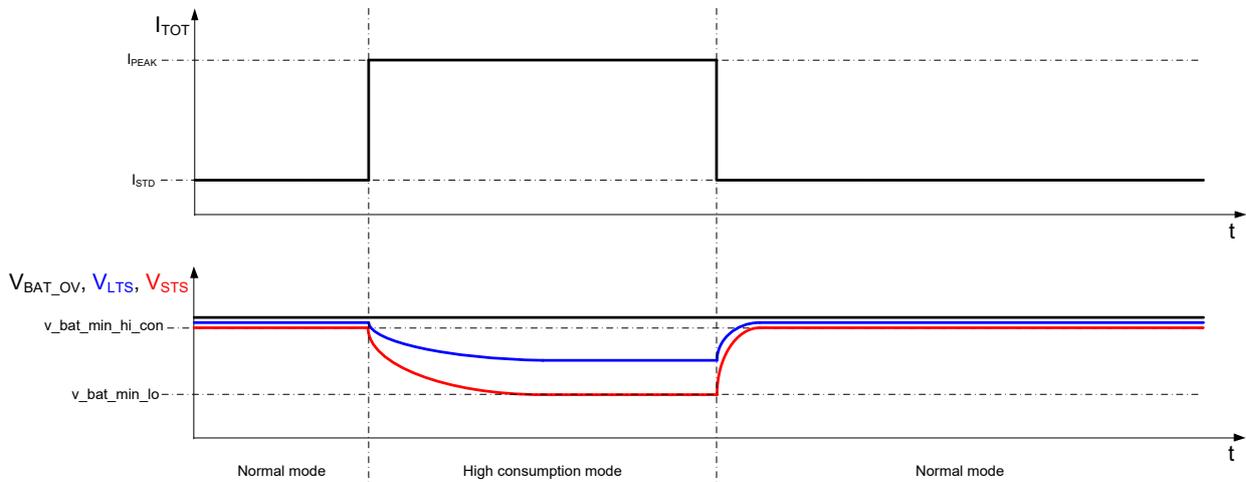


Figure 2: Worst Case Scenario Timing Diagram

The minimum delta between $v_bat_min_hi_con$ and $v_bat_min_lo$ shall follow the following rules:

$$reg_v_bat_min_hi_con \geq \text{trunc} \left(\frac{(I_{PEAK} - I_{STD}) \cdot (R_{BAT} + R_{SW_LTS_STS})}{\min(V_{Ivl})} \right) + reg_v_bat_min_lo + 1$$

Equation 1: reg_v_bat_min_hi_con Calculation

Note: the values of RSW_LTS_STS and V_{Ivl} are in the datasheet in table 4-3.

If the result of that equation is higher than the one calculated by the wizard document, it shall replace it.

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